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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for nonprovisional applications under 37 CFR § 1.53(b))

Attorney Docket No.	660073.774
First Inventor or Application Identifier	Tongbi Jiang
Title	METHOD AND STRUCTURE FOR MANUFACTURING IMPROVED YIELD SEMICONDUCTOR PACKAGED DEVICES
Express Mail Label No.	EM067734873US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Box Patent Application
Assistant Commissioner for Patents
Washington, D.C. 20231

1. [X] General Authorization Form & Fee Transmittal *(Submit an original and a duplicate for fee processing)*
2. [X] Specification [Total Pages] 17
   (preferred arrangement set forth below)
   - Descriptive Title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) *(35 USC 113)* [Total Sheets] 3
4. Oath or Declaration [Total Pages] 1
   - a. [X] Newly executed (original or copy)
   - b. [ ] Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional with Box 17 completed)*
     - i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b)
5. [ ] Incorporation By Reference *(useable if box 4b is checked)* The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered to be part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. [ ] Microfiche Computer Program *(Appendix)*
7. Nucleotide and Amino Acid Sequence Submission *(if applicable, all necessary)*
   - a. [ ] Computer-Readable Copy
   - b. [ ] Paper Copy (identical to computer copy)
   - c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. [X] Assignment Papers (cover sheet & document(s))
9. [X] 37 CFR 3.73(b) Statement *(when there is an assignee)* [X] Power of Attorney
10. [ ] English Translation Document *(if applicable)*
11. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
12. [ ] Preliminary Amendment
13. [X] Return Receipt Postcard
14. [ ] Small Entity Statement(s) [ ] Statement filed in prior application, Status still proper and desired
15. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
16. [X] Other: Certificate of Express Mail
    Check

17. **If a CONTINUING APPLICATION,** *check appropriate box and supply the requisite information below and in a preliminary amendment*

[ ] Continuation [ ] Divisional [ ] Continuation-In-Part (CIP) of prior Application No.: ______

Prior application information: Examiner ______ *Group / Art Unit* ______

[ ] Claims the benefit of Provisional Application No. ______

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Respectfully submitted,

TYPED or PRINTED NAME Kimton N. Eng REGISTRATION NO. 43,605

SIGNATURE [signature] Date July 30, 1999

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METHOD AND STRUCTURE FOR MANUFACTURING IMPROVED YIELD SEMICONDUCTOR PACKAGED DEVICES

TECHNICAL FIELD

The present invention relates to semiconductor packaging, and more particularly, to attaching a semiconductor die in a device package.

BACKGROUND OF THE INVENTION

Semiconductor devices are typically fabricated on thin wafers of silicon. Several dice are produced on each wafer, with each die representing a single semiconductor device. Each die on a wafer is tested for gross functionality, and sorted according to whether the die passes or fails the gross functionality test. After being sorted according to gross functionality, the wafers are cut using a wafer saw, and the individual die are singulated. The die determined to be non-functional are scrapped. The functional die are packaged and further tested to ensure that each packaged device satisfies a minimum level of performance. Typically, the functional devices are permanently packaged by encapsulating the die in a plastic package. Packaging of the functional devices facilitates handling of the devices and also protects the die from damage during the manufacture of circuits using the packaged devices.

There are several conventional structures and methods for packaging singulated die. For example, more common package types include small outline j-bend (SOJ) packages, thin small outline packages (TSOP), and zigzag in-line packages (ZIP). The finished packaged devices are often mounted onto a substrate to form a module. A singulated die is packaged in the aforementioned package types by attaching the die to a lead frame paddle and electrically coupling exposed bond pads of the die to metal leads. The lead frame, die, and a portion of the metal leads are subsequently encapsulated by a plastic resin to protect the integrated circuit from damage. The encapsulated

device is then trimmed from the lead frame and the metal leads formed to the correct shape.

An alternative lead frame structure, known as lead on chip (LOC) may be employed instead of the structure having a lead frame paddle. In an LOC structure, individual metal leads are typically attached to the surface of the die using double-sided adhesive tape having a polyimide base coated on both sides with adhesive material. The metal leads and die are then heated to attach to the adhesive material. The bond pads of the semiconductor die are subsequently wire bonded to a respective metal lead to electrically connect the semiconductor die to receive electrical signals applied to the conductive leads. The LOC lead frame and die are then encapsulated in a plastic resin, then followed by a trim and form process. The LOC structure and packaging process are described in United States Patent No. 4,862,245 to Pashby et al., issued August 29, 1989, and United States Patent No. 4,916,519 to Ward, issued April 10, 1990, which are incorporated herein by reference.

Recently, semiconductor manufacturers have developed a package structure where unpackaged die are mounted directly onto a substrate, for example, a printed circuit board, thus allowing modules to be designed with increased device density. Examples of these types of packages structures include ball grid array (BGA) packages, and other chip scale packages (CSP) having package dimensions that are slightly larger than the dimension of the encapsulated die. The die is mounted onto the substrate and is electrically coupled to conductive traces formed on the substrate by wire bonding the bond pads of the die. Alternatively, the conductive traces and the bond pads may be electrically coupled by using tape automated bonded (TAB) wire instead. The resulting structure is subsequently, partially or entirely, encapsulated to protect the device from damage. External leads, often in the form of solder balls, are then attached to attachment sites on the conductive traces so that the integrated circuit fabricated on the die may be electrically contacted through the external leads.

Following packaging, the device is typically mounted onto a printed circuit board (PCB) as a component in a larger electronic system. Conductive pads on the PCB are positioned to correspond to the location of the external leads of the packaged device. The packaged device is positioned accordingly onto the conductive pads and subjected to a reflow process at an elevated temperature in order to solder the packaged device to the PCB. In the case of a BGA type package, the solder is provided by the solder balls of the completed package.

After the solder has cooled, the packaged device is rigidly attached to the PCB. However, there may be an issue with regards to the reliability of the solder joints as a result of the different expansion rates of the semiconductor die of the packaged device and the PCB to which the packaged device is soldered. The coefficient of thermal expansion (CTE) of the die is typically much lower than that for the PCB. Thus, when the electronic system reaches its operating temperature, the PCB will expand more than the die. The thermal mismatch results in a shearing stress focused at the interface between the packaged device and the PCB, namely, the solder joints. The reliability of the electronic system is compromised when the thermal mismatch stress applied to the solder joints of the packaged device is great enough to cause one of the solder joints to fail.

One method that has been used to alleviate some of the thermal mismatch stress at the solder joint is using a package structure where the die is attached to a flexible substrate using a compliant elastomer pad. Upon reaching operating temperature, the PCB will expand and laterally shift the position of the contact pads with respect to the die. The compliant nature of the elastomer pad allows the solder balls of the packaged device to shift laterally with the expanding PCB. Thus, the different expansion rates of the die in the packaged device, and the PCB to which the packaged device is soldered, is accommodated by the flexible elastomer pad attaching the die to the flexible substrate. However, in the case where TAB wire connections are used in such a package structure to electrically couple the bond pads of the die to the conductive traces

of the substrate, thermal expansion of the elastomer pad creates reliability problems for the packaged device itself. It has been shown in reliability testing that the TAB wire joint is the point most susceptible to failure when the packaged device is subjected to temperature cycle tests (e.g., -65 °C to +150 °C) or high temperature and humidity tests (e.g., 85 °C, 85% RH, alternating bias). Thermal expansion of the elastomer pad laterally shifts the position of the flexible substrate relative to the bond pads of the die. Consequently, the resulting compliant structure places stress at the TAB wire joint where the wire is bonded to the bond pad of the die.

Another method that has been used to minimize thermal mismatch stress between the die and the PCB is to attach the die to a flexible substrate with elastomer posts. One example of this type package is a product developed by Tessera called µBGA®. Viscous elastomer material is screen printed onto the flexible substrate and cured to form the elastomer posts. A dry or wet die attach adhesive is then applied to the end of the cured elastomer in order to attach the die to the elastomer posts. Subsequently, the bond pads of the die are electrically coupled to the conductive traces of the flexible substrate by a TAB wiring process. Although the resulting compliant structure accommodates the different expansion rates of the die and the PCB, the assembly process is time-consuming. Additional assembly steps are required to screen print the viscous elastomer material onto the flexible substrate, to cure the viscous material, and to apply the dry adhesive to the resulting elastomer post. As a result, product throughput at the assembly stage is reduced.

Furthermore, attaching the die to the substrate using elastomer posts requires precision processing to maintain assembly yields. In typical CSP type packages, coplanarity of the die and the substrate should be maintained to ensure that all solder balls contact the PCB upon reflow. Thus, the height of the elastomer posts should be substantially the same in order to achieve the required coplanarity. However, precision processing and equipment is required to achieve this level of consistency. Variations in the screen printing process or in the

attachment of dry adhesive to the elastomer posts may result in unacceptable coplanarity, and consequently, unacceptable packaged devices.

Therefore, there is the need for a method and structure for a semiconductor package that can alleviate thermal mismatch stress without compromising the reliability of the package structure or adding several additional process steps.

SUMMARY OF THE INVENTION

The present invention is directed to a high reliability semiconductor package structure. The package structure is a ball grid array type package that uses a plurality of pieces of adhesive film to attach a semiconductor die to a substrate having conductive traces in order to alleviate thermal mismatch stress between the semiconductor die and the printed circuit board to which the packaged device is soldered, while maintaining the reliability of the packaged device itself.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1A-B is an isometric view of a semiconductor package structure according to an embodiment of the present invention.

Figure 2A-B is a cross-sectional view of alternative embodiments of the semiconductor package structure shown in Figure 1.

Figure 3A-B is a cross-sectional view of the semiconductor package structure shown in Figure 1 and a conventional semiconductor package structure

DETAILED DESCRIPTION OF THE INVENTION

Embodiments of the present invention use a plurality of pieces of adhesive film to attach a semiconductor die to a substrate in a BGA type package. Using multiple pieces of adhesive film alleviates some of the thermal mismatch stress between the semiconductor die and the PCB to which the

packaged device is soldered, while maintaining the reliability of the packaged device itself. As will be illustrated below, the sum change in the length of the pieces of adhesive film will be less than the change in the length of a elastomer pad of a conventional BGA package structure of similar size. Thus, the stress applied to the TAB wire joints caused by thermal expansion will be reduced with respect to the conventional package structure. The pieces of adhesive film are attached to the substrate by pressure bonding, and the die is subsequently pressure bonded to the opposite surface of the pieces of adhesive film. Coplanarity of the die and the substrate is maintained by the substantially uniform thickness of the pieces of adhesive film.

Shown in Figures 1 and 2 is a BGA type package structure 10 according to an embodiment of the present invention. A semiconductor die 12 having an integrated circuit (not shown) and conductive bond pads 14 fabricated on a surface of the die 12 is attached to a substrate 16. The substrate 16 has conductive traces 18, or interconnects, to which the bond pads 14 are coupled. The substrate 16 may be a rigid organic substrate, such as BT resin, or FR-4 or FR-5 material, or a flexible substrate, such as polyimide. A person of ordinary skill in the art will appreciate that the substrate 16 may formed from materials other than those described herein. Consequently, the type of material used for the substrate 16 does not limit the scope of the present invention.

External terminals 20, typically in the form of solder balls, will be formed on the opposite side of the substrate 16 and coupled to a respective conductive trace after the package structure 10 is encapsulated to protect the die 12 and substrate 16 from damage. The substrate 16 serves as an interposer coupling the bond pads 14 of the die 12 attached to one side to the external terminals 20 attached to the opposite side. The solder balls facilitate mounting the resulting packaged device onto a PCB, or similar surface.

A person of ordinary skill in the art will appreciate that the die 12 may be mounted face-up with the surface having the integrated circuit and bond pads 14 facing away from the substrate 16, or face-down so the surface with the

integrated circuit and bond pads 14 are facing the substrate 16. The surface of the die 10 having the integrated circuit typically has a protective layer of polyimide or SiON to prevent the integrated circuit from being damaged during the die singulating process or the die attachment process. The orientation of the die 12 with respect to the substrate 16 will be determined by factors such as the method of bonding to the bond pads 14 or the encapsulation method.

The semiconductor die 12 is attached to the substrate 16 by a plurality of pieces of adhesive film 20a-c. As will be described in more detail below, the adhesive film may be formed from a compliant material. As shown in Figure 1, there are three pieces of adhesive film 20a-c extending substantially the length of the die 12. However, a person of ordinary skill the art will appreciate that two or more pieces of adhesive film may be used to attach the die 12 to the substrate 16. It will also be appreciated that the configuration of the adhesive film is not limited to only single strips extending the length of the die 12 and the substrate 16. For example, each of the single strips may be separated into multiple pieces arranged along the length of the die. Alternatively, the pieces of adhesive film 20a-c may also be arranged at right angles near the corners of the die 12, or oriented to extend across the width of the die 12. Therefore, the number of pieces of adhesive film used to attach the die 12 to the substrate 16, or the particular orientation of the pieces of adhesive film should not limit the scope of the present invention.

The package structure 10 also includes a number of additional components that have been omitted from Figure 1 in the interests of brevity. For example, an encapsulation material that may fill the space remaining between the adhesive film 20a-c, and substantially cover the die 12 and the substrate 16, are not illustrated in Figure 1. However, methods and materials used for completing the assembly of the package structure 10 are well known in the art, and will not be discussed in detail herein.

Shown in Figure 2A-B are alternative embodiments of the pieces of adhesive film that may be used to attach the die 12 to the substrate 16. Figure 2A

illustrates a film 30 consisting of a single layer of elastomer material. No additional layers of adhesive are required for the film 30 because the elastomer material is itself adhesive. The film 30 is pressure bonded to the substrate 16, and then the die 12 is pressure bonded to the film 30. The resulting structure is subjected to a relatively high temperature process to ensure that the die 12 is firmly attached to the substrate 16. As will be explained in greater detail below, the use of multiple pieces of the film 30 to attach the die 12 to the substrate 16 will reduce the stress at the bond wire joint caused by the thermal expansion of the elastomer material.

Figure 2B illustrates a film 40 that may also be used in embodiments of the present invention. The film 40 includes two adhesive layers 42 and 44, and a carrier layer 46. Unlike the elastomer post method, where the elastomer post is formed initially, and an adhesive is applied subsequently, the film 40 is applied to the substrate 16 as a single film. The film 40 is adhered to the substrate 16, and the die 12 is adhered to the film 40 by pressure bonding. The resulting package structure is subsequently heated to firmly attach the die 12 to the substrate 16. Although the carrier layer 46 is shown in figure 2B as consisting of a single layer, a person of ordinary skill in the art will appreciate that the carrier layer 46 may be formed from multiple layers if so desired.

Using either the film 30 or 40 as a means of die attachment provides benefits over the elastomer post method described above. The film 30 or 40 is positioned on and pressure bonded to the substrate 16 using conventional techniques. No additional curing steps or application of adhesives are necessary. Additionally, with regards to the coplanarity of the die 12 and the substrate 16, the films 30 and 40 are not as susceptible to the problems related to coplanarity as the method of screen printing discrete elastomer posts onto the surface of the substrate 16. Consequently, assembly failures related to the coplanarity of the two surfaces may be reduced when multiple pieces of the film 30 or 40 are used for die attachment.

Shown in Figure 3A-B are cross-sectional views of the package structure 10 of Figure 1, and a conventional package structure 110 having an elastomer pad 120 attaching the die 12 to the substrate 16. The thermal expansion for the multiple pieces of adhesive film 20a-c and the elastomer pad 120 are both governed by the following equation:

$$\Delta l = \alpha \, \Delta T \, l_0$$

where Δl is the change in the length of the material, α is the coefficient of thermal expansion (CTE) of the material, ΔT is the change in temperature, and l_0 is the original length of the material at room temperature. For the purposes of illustration, assume that the same elastomer material is used for the elastomer pad 120 and the multiple pieces of adhesive film 20a-c, and that both structures are subjected to the same change in temperature. Consequently, the only difference between the change in length for the elastomer pad, Δl_{pad}, and for the multiple pieces of elastomer, $\Delta l_{multiple}$, is the original length of the corresponding elastomer pad, $l_{0,\,pad}$ and $l_{0,\,multiple}$. The $l_{0,\,pad}$ is the width of the elastomer pad 120, and the $l_{0,\,multiple}$ is the sum of the individual widths of pieces 20a-c, $l_{0,\,20a}$, $l_{0,\,20b}$, and $l_{0,\,20c}$, respectively. As illustrated by Figure 2A-B, $l_{0,\,pad} > l_{0,\,multiple}$, and therefore, $\Delta l_{pad} > \Delta l_{multiple}$. Thus, any stress applied to the wire bond joint due to the thermal expansion of the elastomer pad 120 may be reduced by using multiple pieces of elastomer film 20a-c.

From the foregoing it will be appreciated that, although specific embodiments of the invention have been described herein for purposes of illustration, various modifications may be made without deviating from the spirit and scope of the invention. For example, each of the embodiments described previously may be simultaneously performed on several substrates 16 connected in strip form to facilitate the mass production of the packaged devices. The individual packaged devices may be singulated following solder ball attachment. Accordingly, the invention is not limited except as by the appended claims.

CLAIMS

1. A semiconductor device package, comprising:

a semiconductor die having a first surface on which an integrated circuit and at least one electrically conductive bond pad are fabricated;

at least one electrically conductive external terminal;

an interposer having a die attach surface and an external surface opposite of the die attach surface disposed in between the semiconductor die and the at least one external terminal, the interposer having at least one electrically conductive interconnect electrically coupling the at least one bond pad of the semiconductor die positioned adjacent to the die attach surface to the at least external terminal positioned adjacent to the external surface; and

a plurality of pieces of adhesive film disposed in between the semiconductor die and the interposer to adhere the semiconductor die to the die attach surface of the interposer.

2. The package of claim 1, further comprising an encapsulating material substantially filling regions remaining in between the semiconductor die and the interposer.

3. The package of claim 1 wherein the interposer comprises a flexible material.

4. The package of claim 1 wherein the plurality of pieces of adhesive material comprises a compliant material.

5. The package of claim 1 wherein each of the plurality of pieces of adhesive film comprises:

a first adhesive layer adhered to the die attach surface of the interposer;

a second adhesive layer adhered to the semiconductor die; and

at least one carrier layer disposed in between the first and second adhesive layers and to which the first and second adhesive layers are adhered.

6. The package of claim 1 wherein each of the plurality of pieces of adhesive film comprises a single layer of elastomer material.

7. The package of claim 1 wherein the first surface of the semiconductor die is adhered to the die attach surface of the interposer by the plurality of pieces of adhesive film.

8. The package of claim 1 wherein the at least one electrically conductive external terminal comprises a solder ball.

9. The package of claim 1 wherein the plurality of pieces of adhesive film comprise strips of adhesive film positioned in parallel along a longitude of the semiconductor die.

10. The package of claim 1 wherein a first and a second of the plurality of pieces of adhesive film are positioned at a right angle with respect to each other.

11. A device package assembly for a semiconductor die being constructed from a process comprising:

laminating a plurality of pieces of adhesive film to an interposer having at least one electrically conductive interconnect, the interposer further having a die attach surface to which the semiconductor die is attached, and an external surface opposite of the die attach surface;

attaching to the interposer the semiconductor die having a first surface on which an integrated circuit and at least one electrically conductive bond pad are fabricated; and

bonding the at least one electrically conductive interconnect to the at least one electrically conductive bond pad.

12. The package assembly of claim 11 wherein the process further comprises substantially filling regions remaining in between the semiconductor die and the interposer with an encapsulating material.

13. The package assembly of claim 11 wherein the process further comprises attaching an external terminal to the at least one electrically conductive interconnect adjacent to the external surface of the interposer.

14. The package assembly of claim 13 wherein the external terminal comprises a solder ball.

15. The package assembly of claim 11 wherein the interposer comprises a flexible material.

16. The package assembly of claim 11 wherein each of the plurality of pieces of adhesive film comprises a compliant material.

17. The package assembly of claim 11 wherein each of the plurality of pieces of adhesive film comprises a single layer of elastomer material.

18. The package assembly of claim 11 wherein the plurality of pieces of adhesive film comprise strips of film positioned in parallel along a longitude of the semiconductor die.

19. A method for reducing thermal mismatch stress in a semiconductor device package for a semiconductor die having an integrated circuit and at least one electrically conductive bond pad, the method comprising adhering the

semiconductor die to a die attach surface of an interposer by using a plurality of pieces of adhesive film disposed therebetween, the interposer having at least one conductive interconnect electrically coupled to the bond pad, and further having an external surface opposite of the die attach surface and to which an external terminal electrically coupled to the conductive interconnect is adjacent.

20. The method of claim 19, further comprising substantially filling regions remaining in between the semiconductor die and the interposer with an encapsulating material and covering the at least one conductive interconnect.

21. The method of claim 19 wherein the interposer comprises a flexible material.

22. The method of claim 19 wherein each of the plurality of pieces of adhesive film comprises a compliant material.

23. The method of claim 19 wherein each of the plurality of pieces of adhesive film comprises:

a first adhesive layer adhered to the die attach surface of the interposer;

a second adhesive layer adhered to the semiconductor die; and

at least one carrier layer disposed in between the first and second adhesive layers.

24. The method of claim 19 wherein each of the plurality of pieces of adhesive film comprises a single layer of elastomer.

25. The method of claim 19 wherein the external terminal comprises a solder ball.

26. A method for packaging a semiconductor device, comprising:

laminating a plurality of pieces of compliant adhesive film to an interposer having at least one electrically conductive interconnect, the interposer further having a die attach surface to which a semiconductor die is attached, and an external surface opposite of the die attach surface;

attaching to the interposer the semiconductor die having a first surface on which an integrated circuit and at least one electrically conductive bond pad are fabricated; and

bonding the at least one electrically conductive interconnect to the at least one electrically conductive bond pad.

27. The method of claim 26, further comprising substantially filling regions remaining in between the semiconductor die and the interposer with an encapsulating material and covering the at least one conductive interconnect.

28. The method of claim 26 wherein the interposer comprises a flexible material.

29. The method of claim 26 wherein each of the plurality of pieces of compliant adhesive film comprises:

a first adhesive layer adhered to the die attach surface of the interposer;

a second adhesive layer adhered to the semiconductor die; and

at least one carrier layer disposed in between the first and second adhesive layers.

30. The method of claim 26 wherein each of the plurality of pieces of compliant adhesive film comprises a single layer of elastomer.

31. The method of claim 26, further comprising attaching a solder ball to the at least one electrically conductive interconnect adjacent to the external surface of the interposer.

32. A method for packaging a semiconductor device, comprising:

laminating a plurality of pieces of compliant adhesive film to a semiconductor die having a first surface on which an integrated circuit and at least one electrically conductive bond pad are fabricated;

attaching to the semiconductor die an interposer having at least one electrically conductive interconnect, the interposer further having a die attach surface to which a semiconductor die is attached, and an external surface opposite of the die attach surface; and

bonding the at least one electrically conductive interconnect to the at least one electrically conductive bond pad.

33. The method of claim 32, further comprising substantially filling regions remaining in between the semiconductor die and the interposer with an encapsulating material and covering the at least one conductive interconnect.

34. The method of claim 32 wherein the interposer comprises a flexible material.

35. The method of claim 32 wherein each of the plurality of pieces of compliant adhesive film comprises:

a first adhesive layer adhered to the die attach surface of the interposer;

a second adhesive layer adhered to the semiconductor die; and

at least one carrier layer disposed in between the first and second adhesive layers.

36. The method of claim 32 wherein each of the plurality of pieces of compliant adhesive film comprises a single layer of elastomer.

37. The method of claim 32, further comprising attaching a solder ball to the at least one electrically conductive interconnect adjacent to the external surface of the interposer.

METHOD AND STRUCTURE FOR MANUFACTURING IMPROVED YIELD SEMICONDUCTOR PACKAGED DEVICES

ABSTRACT OF THE DISCLOSURE

A semiconductor package structure for a ball grid array type package using a plurality of pieces of adhesive elastomer film to attach a semiconductor die to a substrate having conductive traces in order to alleviate thermal mismatch stress between the semiconductor die and the printed circuit board to which the packaged device is soldered, while maintaining the reliability of the packaged device itself.

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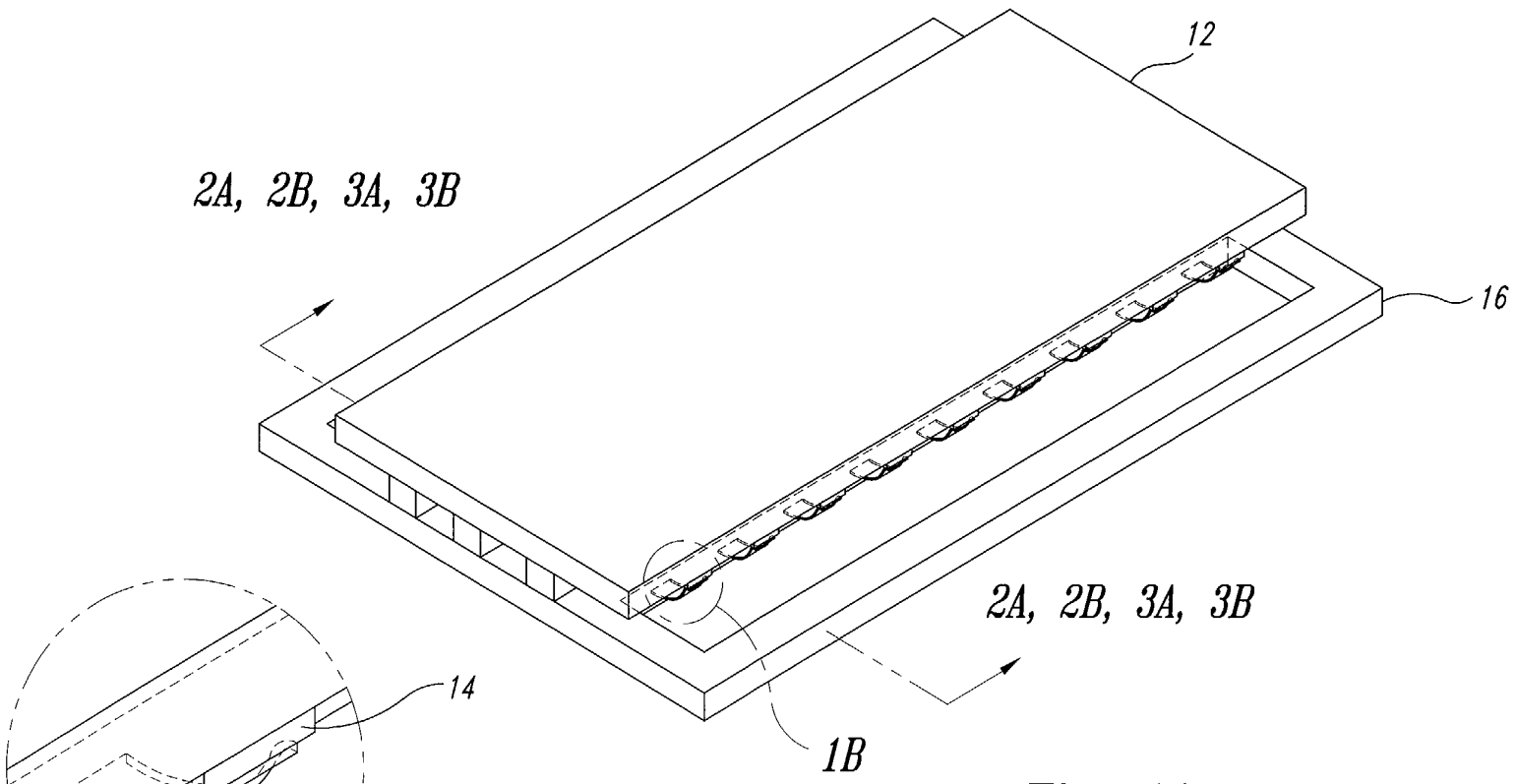


Fig. 1A

Fig. 1B

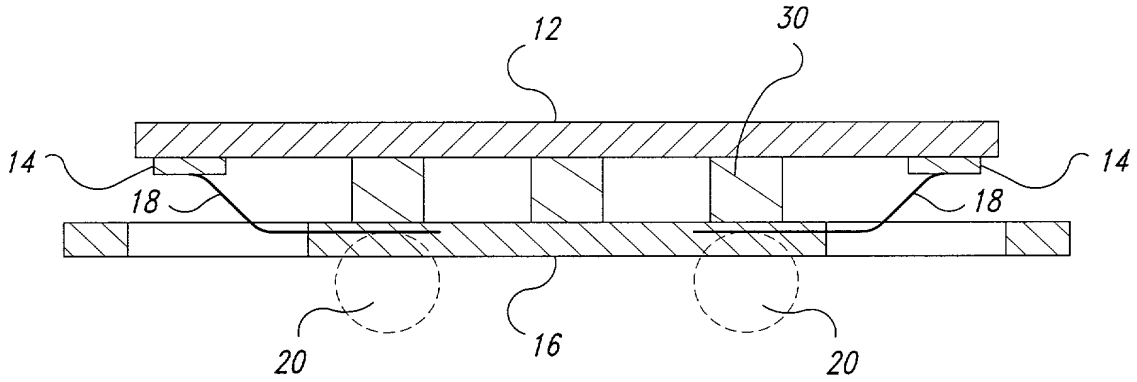


Fig. 2A

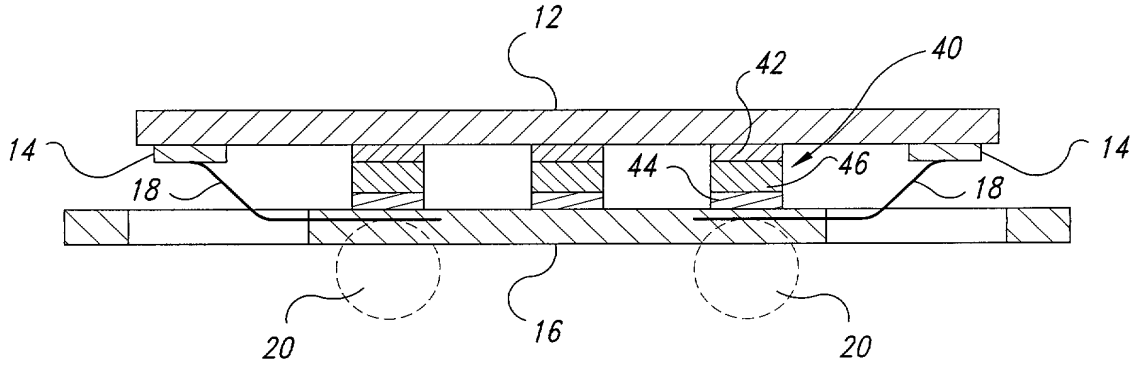
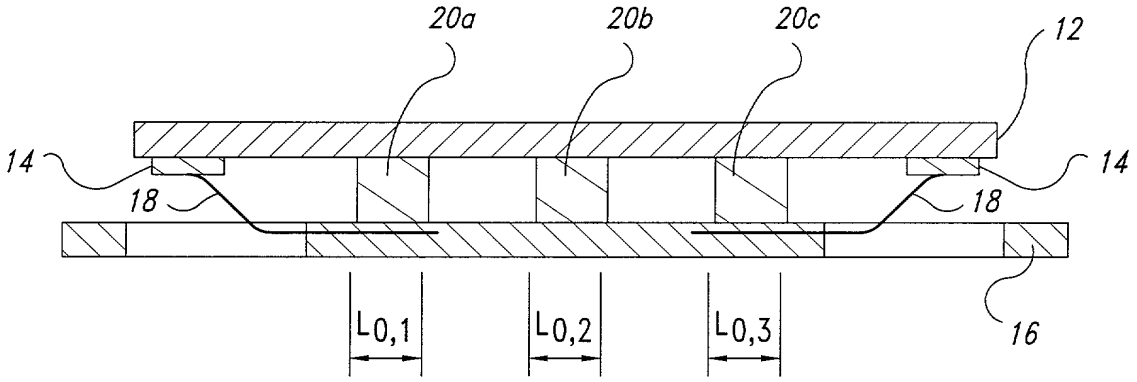


Fig. 2B



$L_{0,\ MULTIPLE} = L_{0,1} + L_{0,2} + L_{0,3}$

Fig. 3A

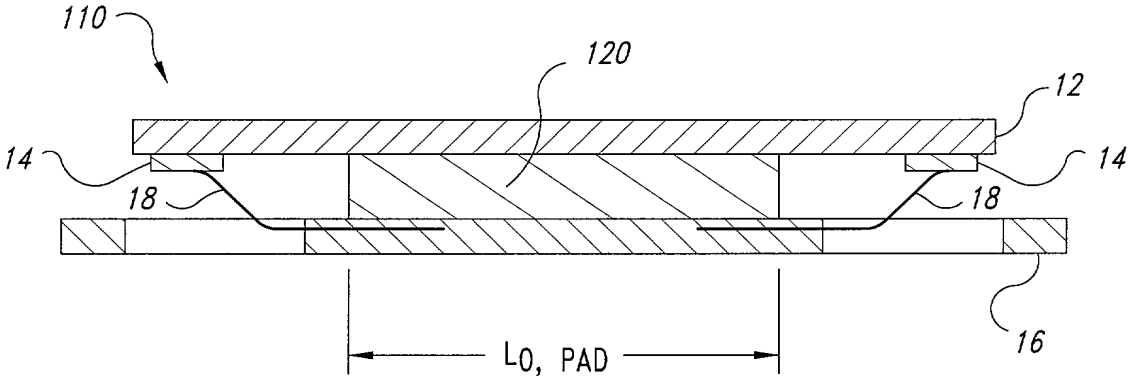


Fig. 3B
(Prior Art)

DECLARATION

As the below-named inventor, I declare that:

My residence, post office address, and citizenship are as stated below under my name.

I believe I am the original, first, and sole inventor of the invention entitled "METHOD AND STRUCTURE FOR MANUFACTURING IMPROVED YIELD SEMICONDUCTOR PACKAGED DEVICES," which is described and claimed in the foregoing specification and for which a patent is sought.

I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment specifically referred to herein (if any).

I acknowledge my duty to disclose information of which I am aware which is material to patentability and examination of this application in accordance with 37 C.F.R. § 1.56(a).

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further, that these statements were made with the knowledge that the making of willfully false statements and the like is punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and may jeopardize the validity of any patent issuing from this patent application.

Tongbi Jiang

Date 7/28/99

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Tongbi Jiang
Filed	:	Concurrently herewith
For	:	**METHOD AND STRUCTURE FOR MANUFACTURING IMPROVED YIELD SEMICONDUCTOR PACKAGED DEVICES**

Docket No. : 660073.774

Box Patent Application
Assistant Commissioner for Patents
Washington, DC 20231

ELECTION UNDER 37 C.F.R. §§ 3.71 AND 3.73 AND POWER OF ATTORNEY

Sir:

The undersigned, being Assignee of the entire interest in the above-identified application by virtue of an Assignment filed concurrently herewith, hereby elects, under 37 C.F.R. § 3.71, to prosecute the application to the exclusion of the inventor.

Assignee hereby appoints RICHARD W. SEED, Reg. No. 16,557; ROBERT J. BAYNHAM, Reg. No. 22,846; EDWARD W. BULCHIS, Reg. No. 26,847; GEORGE C. RONDEAU, JR., Reg. No. 28,893; DAVID H. DEITS, Reg. No. 28,066; WILLIAM O. FERRON, JR., Reg. No. 30,633; PAUL T. MEIKLEJOHN, Reg. No. 26,569; DAVID J. MAKI, Reg. No. 31,392; RICHARD G. SHARKEY, Reg. No. 32,629; DAVID V. CARLSON, Reg. No. 31,153; KARL R. HERMANNS, Reg. No. 33,507; DAVID D. MCMASTERS, Reg. No. 33,963; MICHAEL J. DONOHUE, Reg. No. 35,859; CHRISTOPHER J. DALEY-WATSON, Reg. No. 34,807; STEVEN D. LAWRENZ, Reg. No. 37,376; ROBERT G. WOOLSTON, Reg. No. 37,263; ELLEN M. BIERMAN, Reg. No. 38,079; PAUL T. PARKER, Reg. No. 38,264; ANN T. KADLECEK, Reg. No. 39,244; DAVID W. PARKER, Reg. No. 37,414; BRIAN G. BODINE, Reg. No. 40,520; FRANK ABRAMONTE, Reg. No. 38,066; E. RUSSELL TARLETON, Reg. No. 31,800; KEVIN S. COSTANZA, Reg. No. 37,801; DALE C. BARR, Reg. No. 40,498; KEVIN S. ROSS, Reg. No. 42,116; JOHN M. WECHKIN, Reg. No. 42,216; THOMAS E. LOOP, Reg. No. 42,810;

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Pursuant to 37 C.F.R. § 3.73, the undersigned duly authorized designee of Assignee certifies that the evidentiary documents have been reviewed, specifically the Assignment to MICRON TECHNOLOGY, INC., filed concurrently herewith for recording, a copy of which is attached hereto, and certifies that to the best of my knowledge and belief, title remains in the name of the Assignee.

MICRON TECHNOLOGY, INC.
ASSIGNEE

July 25, 1995
DATE

Michael L. Lynch
Chief Patent Counsel

Enclosure:
Copy of Assignment